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A New Overlap Current Restraining Method for Current-source Rectifier

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Abstract

To ensure a DC current path and avoid large voltage overshoot of the DC-link inductor, alternating PWM pulses in the current-source rectifier should be supplemented by overlap time, which generates an overlap current and causes input current distortion. In this study, the influence of overlap time is illustrated by comparing the AC-side current before and after overlap time is added. The overlap current distribution caused by overlap time is discussed under different modulation carriers, including triangle carrier, positive-going carrier, and negative-going carrier. The quantitative relationship between the extra harmonics of the AC-side current and overlap time is based on the Fourier analysis. Based on the commutation analysis, a new carrier modulation scheme that can restrain overlap current is proposed. A 3 kW prototype is established to verify the effectiveness of the influence of overlap time and the proposed restraining modulation scheme.

Key words: Current-source rectifier, Grid current, Overlap current harmonics, Overlap time, Restraining method

I. INTRODUCTION

Power grid harmonics is one of the most pressing issues of the modern power system. The PWM rectifier is an effective solution to reduce harmonics and achieve high power factor. On the basis of the characteristics of the DC-link power supply, the PWM rectifier can be divided into voltage-source rectifier (VSR) and current-source rectifier (CSR) [1]-[4]. Although VSR is widely applied in industry, CSR has its advantages in its own application areas. Compared with VSR, CSR features a step-down function, smaller filter size, in-rush current limiting capability, and better direct current control, reliability, and protection, resulting in its wide use in four-quadrant motor drive systems, new energy power generation systems, superconducting rectifier system systems, and data centers [5]-[8].

Setting the dead time for alternating pulses is necessary to avoid the shoot-through in any arm of the VSR [9], [10]. Similarly, the CSR is required to add the overlap time to PWM signals to prevent DC current interruption [11]-[14].

As pointed out in [15]-[17], overlap time causes errors in the current control and changes the pulse width of the AC-side current, which increases the low-order harmonics in the input current and influences device selection [20]-[22]. Therefore, the current ripple should be restricted within a certain range.

A compensation method for the overlap time is proposed in [23]. Overlap time is added to the gate signal of the switch that bears a reverse voltage. Transition time is assumed to be very short and can be omitted. However, transition time is long when the device voltage crosses zero or the DC current is low at a light load. In that case, the compensation method will not work.

The scheme of low-voltage stress space vector PWM control for current-source PWM rectifiers is proposed in [24]. Although this scheme can keep switches in a natural commutation state, [24] does not provide an analysis of the influence of overlap time on the non-natural commutation process.

To restrain the current ripple caused by overlap time, a new overlap time compensation method that modulates the PWM carrier according to neutral voltages of phase legs is proposed in this study. Compared with the traditional scheme, the new compensation method adopts a sawtooth carrier

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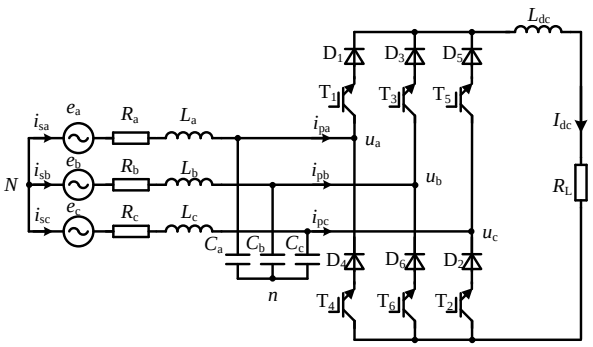

Fig. 1. Topology of the three-phase current-source PWM rectifier.

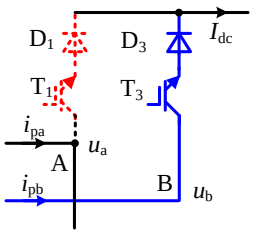

Fig. 2. Current commutation from T_1 to T_3.

instead of the traditional triangle carrier, making it flexible and effective in reducing the overlap current in a non-natural commutation process [25]. To illustrate the new compensation method further, detailed commutation processes with positive-going and negative-going sawtooth carriers are described separately. The proposed carrier modulation method is verified through simulation and experiments in a 3 kW all-SiC buck rectifier, which proves that the new modulation method is effective in the non-natural commutation process, and the overlap current can be reduced greatly with a suitable PWM carrier.

This paper is structured as follows. In Section II, the traditional commutation process with a triangle carrier is analyzed, and the overlap current distribution is listed to explain the influence of overlap time. The quantitative relationship between overlap time and grid current harmonics is also deduced based on the pulse equivalent principle. Section III introduces the sawtooth carrier modulation scheme to restrain the influence of overlap time. Finally, a 3 kW prototype is built to prove the effectiveness of the theoretical analysis and the proposed carrier modulation scheme.

II. Influence of Overlap Time on the Grid-Side Current

A. CSR Commutation Analysis

Fig. 1 shows the topology of CSR, where a transistor is in series with a diode to block the voltage in both directions. The e_x(x=a, b, c) is the voltage of the three-phase voltage source, and u_x is the neutral potential of the phase leg. i_{sx} is the grid-side current, and i_{px} is the AC-side current. The

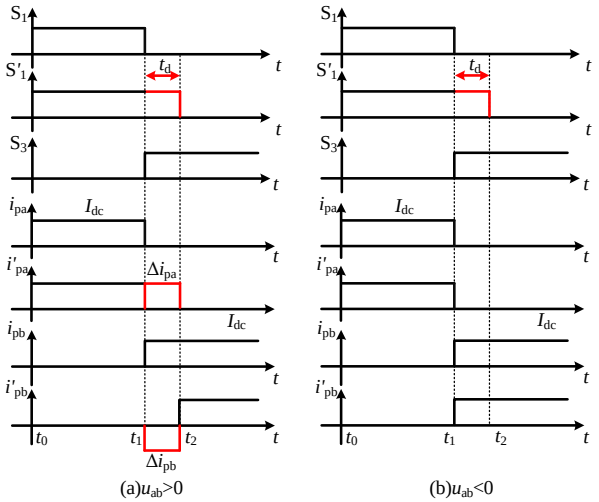

Fig. 3. AC-side current during commutation operation from T_1 to T_3 with overlap time.

AC-side filter is composed of L_x and C_x. T_i and D_i (i=1, 2, ... , 6) represent the switches of the converter. L_{dc} is the DC-link inductor, and R_L is the load.

Ensuring a DC current path is compulsory because the inductor is adopted as the DC-link filter of the CSR.

Therefore, the commutation in the CSR happens between one of the switches in the three upper legs and one switch in the three lower legs. To keep a DC current loop, the signal to turn off the switch should be delayed for a period of time t_d, which is called the overlap time. During overlap time t_d, both the switches to be turned on and off are driven simultaneously by PWM pulses.

To assess the effect of overlap time on the grid-side current, the switching process from switch T_1 to switch T_3 is analyzed. The derivation of the commutation cell is shown in Fig. 2. This study assumed that the PWM signals are ideal and the switching process is instantaneous. Fig. 3 shows the waveform of current commutation from T_1 to T_3. S_1 and S_3 are the PWM signals without overlap time, and S_1' denotes the PWM signals with added overlap time. i_{pa} and i_{pb} are the AC-side current of Phase A and Phase B without overlap time, respectively. The i'_{pa} and i'_{pb} are the AC-side current with overlap time. The Δi_{pa} and Δi_{pb}, called overlap currents, are the differences of the AC-side with and without overlap time ($\Delta i_{pa}=i'_{pa}-i_{pa}$, $\Delta i_{pb}=i'_{pb}-i_{pb}$).

In simplifying the switching process analysis, the midpoint voltage of the phase leg u_x(x=a,b,c) can be neglected because the forward voltage across switch T_1 and diode D_1 is considerably lower than u_{ba}, $u_{ba}=u_b-u_a$. Before the moment t_1, switch T_1, and diode D_1 are in the conducting state. At t_1, overlap time t_d occurs between switches T_1 and T_3. Therefore, the conduction states of the switches T_1 and T_3 depend on the voltage across diode D_3, which is u_{ba}. When the voltage across D_3 is positive, switch T_3 is turned on at t_1. Otherwise, switch T_3 will be turned on until overlap time t_d is over

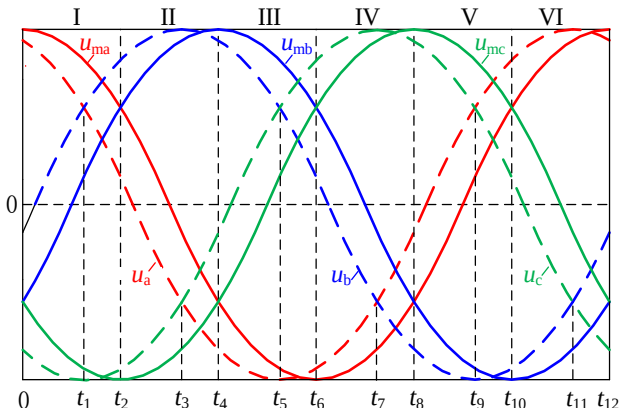

Fig. 4. Theoretical modulation waveform and neutral voltage waveform of each phase leg.

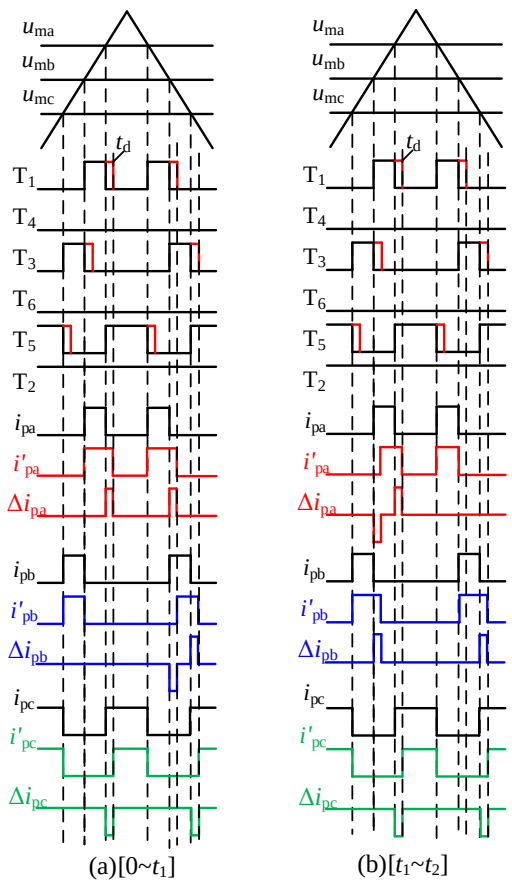

Fig. 5. Current commutation in sector I (triangle carrier).

because the voltage across D_3 is negative.

According to the neutral voltage of u_a and u_b, the commutation operation from T_1 to T_3 can be divided into two cases:

1) When u_a>u_b

As shown in Fig. 3(a), during t_1, diode D_3 bears the reverse voltage u_{ba}. Therefore, during overlap time t_d=t_1-t_2, the DC current cannot flow through T_3 and continues to flow through T_1, which generates the negative overlap current Δi_{pb}.

2) When u_a<u_b

During t_1, specifically u_{ba}>0, diode D_3 is under forward bias at t_1 and switch T_3 can be turned on immediately. Overlap time has no influence on the communication process and will not produce an overlap current, which can be seen in Fig. 3(b).

B. Overlap Current Distribution

To obtain the overlap current distribution, the switching period is divided into six sectors according to the modulation signals u_{ma}, u_{mb}, and u_{mc}. The commutation sequence among switches is identical in the same sector. Furthermore, the existence of an overlap current depends on the voltage across the diode to be turned on, which is the difference between bridge phase voltages u_x. Theoretically, an angle offset exists between midpoint voltage u_x and modulation signal u_{mx} [23]. Therefore, two-bridge phase voltage distributions are present in each sector, and the modulation period can be further subdivided into 12 sectors (Fig. 4).

Take Sector I interval [t_0, t_2] as an example. As u_{ma}>u_{mb}>u_{mc}, the switching sequence is (T_5, T_2)→ (T_3, T_2)→ (T_1, T_2)→ (T_5, T_2)→ (T_1, T_2)→ (T_3, T_2)→ (T_5, T_2), wherein (T_x, T_y) is the commutation from T_x to T_y. According to the relationship among the neutral potential of the phase legs, Sector I can be subdivided into two intervals, [t_0, t_1] and [t_1, t_2]. The relationship of the neutral potential is u_a>u_b>u_c in [t_0, t_1] and u_b>u_a>u_c in [t_1, t_2]. Therefore, the current distribution should be analyzed in two cases in Sector I, namely, u_a>u_b>u_c and u_b>u_a>u_c.

In interval [t_0, t_1], the first commutation is from T_5 to T_3. During overlap time, switch T_3 and the PWM signal of switch T_5 are turned on. The voltage across diode D_3 is u_{bc}, which changes in different intervals. In interval [t_0, t_1], diode D_3 is in positive bias due to u_b>u_c. Therefore, the current flows immediately from T_5 to T_3. T_3 is turned on and does not produce the overlap current. The next commutation is from switch T_3 to switch T_1. During overlap time, switches T_1 and T_3 are turned on. The voltage across diode D_1 is u_{ab}, which is positive in interval [t_0, t_1]. Therefore, the current flows immediately from T_3 to T_1 when T_1 is turned on and does not produce an overlap current.

The third commutation is from T_1 to T_5. Similarly, the voltage across diode D_5 is u_{ca}, which is negative in interval [t_1, t_2]. With diode D_5 in reverse bias, diode D_5 is turned off during overlap time, and no current flows through switch T_5. Compared with the ideal commutation process, the turn on time in Phase A is the added overlap time t_d, while the turn on time in Phase b is the reduced overlap time t_d. Therefore, the overlap currents Δi_{pa} in Phase A and Δi_{pb} in Phase B are produced, as seen in Fig. 5(a). In a similar way, the commutation process with overlap time in Fig. 5(b) can be analyzed without the process being described in detail.

For convenient analysis, the commutation process in Sector

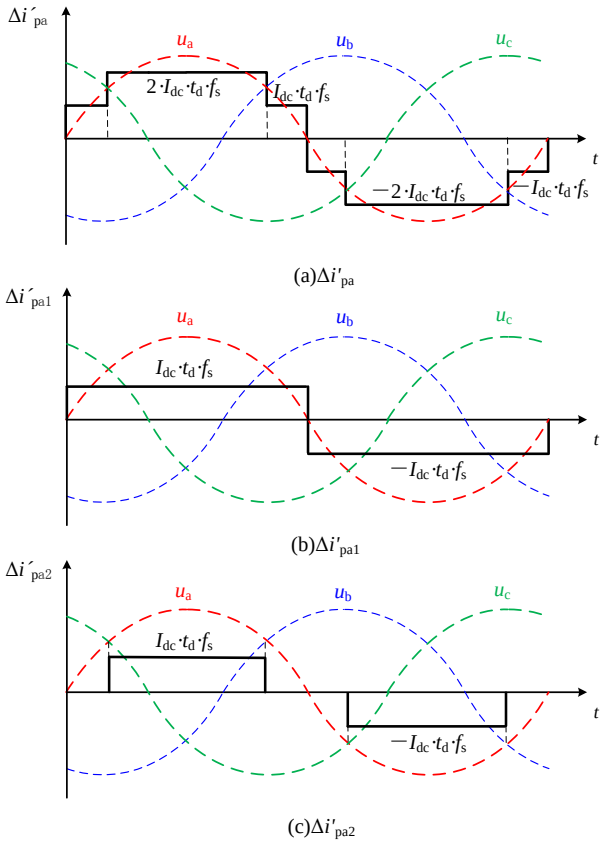

Fig. 6. Equivalent waveform of overlap current in Phase A.

TABLE I
OVERLAP CURRENT DISTRIBUTION IN [0-T1] (TRIANGLE CARRIER)

Commutation	Diode to be turned on	Overlap current	Waveform of overlap current
$T_5 \rightarrow T_3$	$D_3: u_{bc}>0$	no	no
$T_3 \rightarrow T_1$	$D_1: u_{ab}>0$	no	no
$T_1 \rightarrow T_5$	$D_5: u_{ca}<0$	Δi_{pa} Δi_{pc}	
$T_5 \rightarrow T_1$	$D_1: u_{ac}>0$	no	no
$T_1 \rightarrow T_3$	$D_3: u_{ba}<0$	Δi_{pa} Δi_{pb}	
$T_3 \rightarrow T_5$	$D_5: u_{cb}<0$	Δi_{pb} Δi_{pc}	

TABLE II
OVERLAP CURRENT DISTRIBUTION IN [T_1-T_2] (TRIANGLE CARRIER)

Commutation	Diode to be turned on	Overlap current	Waveform of overlap current
$T_5 \rightarrow T_3$	$D_3: u_{bc}>0$	no	no
$T_3 \rightarrow T_1$	$D_1: u_{ab}<0$	Δi_{pb} Δi_{pa}	
$T_1 \rightarrow T_5$	$D_5: u_{ca}<0$	Δi_{pa} Δi_{pc}	
$T_5 \rightarrow T_1$	$D_1: u_{ac}>0$	no	no
$T_1 \rightarrow T_3$	$D_3: u_{ba}>0$	no	no
$T_3 \rightarrow T_5$	$D_5: u_{cb}<0$	Δi_{pb} Δi_{pc}	

I is listed in Table 1 ([t_0~t_1]) and Table 2 ([t_1~t_2]). The commutation operation in other sectors can be obtained in a similar way. The characteristics of the overlap current can be obtained based on the commutation analysis in Sector I, where (1) the existence of overlap currents is determined by the voltage across the diode to be conducted, (2) the carrier is symmetrical in a switching cycle, and (3) overlap currents are shown in a positive–negative pair.

C. Harmonic Analysis of the AC-side Current

Dead time in the VSR influences the output voltage [24]. Similarly, overlap time in the CSR produces extra harmonic components in the AC-side current.

In interval [0, t_1], the overlap time will lead to two positive overlap currents in the grid side of Phase A. According to the principle of equivalent impulse, overlap currents can be replaced by the square wave when they have the same area. The amplitude of a square wave can be expressed as

$$\Delta i'_{pa} = \frac{2 \cdot I_{dc} \cdot t_d}{T_c} = 2 \cdot I_{dc} \cdot t_d \cdot f_s, \quad (1)$$

where T_c is the period of the carrier wave, I_{dc} is the DC current, t_d is the overlap time, and f_s is the frequency of the carrier wave.

In intervals [t_1, t_3] and [t_7, t_9], two overlap currents occur in pairs, one positive current and one negative current, which can be expressed as

$$\Delta i'_{pa} = \begin{cases} I_{dc} \cdot t_d \cdot f_s & (u_{an} > 0) \\ -I_{dc} \cdot t_d \cdot f_s & (u_{an} < 0) \end{cases}. \quad (2)$$

Similarly, the equivalent square wave of the overlap current in [t_3, t_7] can be expressed as

$$\Delta i'_{pa} = -2 \cdot I_{dc} \cdot t_d \cdot f_s. \quad (3)$$

In [t_9, t_{12}], the expression of the equivalent square wave is shown in Formula (1).

Fig. 6 is the equivalent waveform of overlap time based on the above analysis. Fig. 6(a) is the equivalent square wave of the overlap current in Phase A, $\Delta i'_{pa}$, which is obtained from (1) to (3). The $\Delta i'_{pa}$ can be further divided into two parts, as shown in Figs. 6(b) and 6(c). The overlap current can be analyzed by comparing neutral voltages of the related phase legs. Therefore, when $u_a > u_b$ and $u_a > u_c$, the overlap current is high. When $u_a < u_b$ and $u_a < u_c$, a high negative overlap current exists. When u_a is between u_b and u_c, the overlap current will change from a positive value to a negative value or in reverse depending on the sign of u_a.

According to Fig. 6 and (1), (2), (3), the equivalent overlap current $\Delta i'_{pa}$ can be expressed as

$$\Delta i'_{pa} = \Delta i'_{pa1} + \Delta i'_{pa2}, \quad (4)$$

and

$$\Delta i'_{pa1} = \text{sign}(u_a) \cdot I_{dc} \cdot t_d \cdot f_s, \quad (5)$$

where

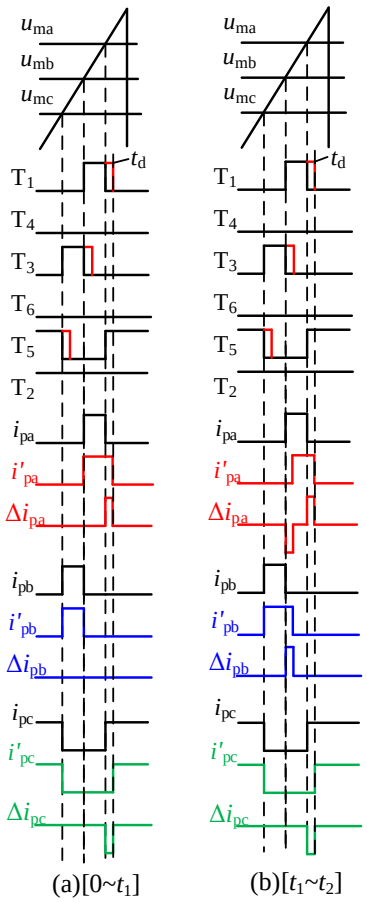

Fig. 7. Current commutation in Sector I (positive-going sawtooth carrier).

$$\mathrm{sign}(u_a)=\begin{cases}1 & (u_a>0)\\ -1 & (u_a<0)\end{cases}, \tag{6}$$

and

$$\Delta i'_{pa2}=\begin{cases} I_{dc}\cdot t_d\cdot f_s & (\frac{\pi}{6}<t<\frac{5\pi}{6})\\ -I_{dc}\cdot t_d\cdot f_s & (\frac{7\pi}{6}<t<\frac{11\pi}{6})\end{cases}. \tag{7}$$

The waveforms of $\Delta i'_{pa1}$ and $\Delta i'_{pa2}$ are shown in Figs. 6(b) and 6(c) separately. Through Fourier decomposition, (4) can be decomposed into

$$\begin{aligned}\Delta i'_{pa}=&\frac{4\cdot I_{dc}\cdot t_d\cdot f_s}{\pi}(\sin\omega t+\frac{1}{3}\sin 3\omega t+\frac{1}{5}\sin 5\omega t+\cdots)\\ &+\frac{4\cdot I_{dc}\cdot t_d\cdot f_s}{\pi}\cdot\frac{\sqrt{3}}{2}(\sin\omega t-\frac{1}{5}\sin 5\omega t-\frac{1}{7}\sin 7\omega t\cdots).\end{aligned} \tag{8}$$

Extra odd harmonics in the overlap current can be found in (8) in addition to the fundamental component. The harmonic content is proportional to f_s, t_d, and I_{dc} and inversely proportional to the harmonic frequency. Therefore, the overlap current will bring odd harmonics to the AC-side current.

Although there are LC filters in a three-phase CSR, the resonant frequency is usually lower than the switching frequency and higher than the grid frequency. For example, in the design of LC filters, the inductance L_x is set to 1.7 mH, and the capacitance C_x is set to 10 μF at 10 kHz switching frequency (x=a,b,c), and the corresponding resonant frequency is equal to 1220 Hz. The LC filter can effectively filter out high-order harmonics near the switching frequency. The third, fifth, and seventh harmonics of the switching frequency cannot be filtered out by the LC filter. When the AC-side current flows through the LC filters, the low-frequency current harmonics are amplified, which distorts the grid-side current. Therefore, taking measures to prevent the occurrence of AC-side harmonics caused by an overlap current is necessary.

III. Method for Restraining the Overlap Current

A. Commutation with Positive-going Sawtooth Carrier

The switching sequence is symmetric in a carrier period because the adopted carrier is a triangle wave in the above analysis. For example, the current commutation process in Sector I is as follows: $T_5\rightarrow T_3\rightarrow T_1\rightarrow T_5\rightarrow T_1\rightarrow T_3\rightarrow T_5$.

The symmetric commutation process means that overlap currents only exist in half of the switching cycle and not the whole switching cycle. When the PWM carrier is a positive-going sawtooth carrier, which is asymmetric, the symmetric commutation process will not occur.

Take Sector I as an example. When the carrier is replaced by a positive slope sawtooth wave (Fig. 7), the distribution of the overlap current will be different from the distribution in Fig. 5(a). The existence of the overlap current is dependent on whether the voltage sign of the diode is turned on or not. Therefore, according to the relationship of phase bridge voltages in [t_0, t_1] and in [t_1, t_2], the commutation operation in Sector I should be discussed in two cases, $u_a>u_b>u_c$ and $u_b>u_a>u_c$.

In interval [t_0, t_1], the first commutation is from T_5 to T_3. During this commutation, diode D_3 is in positive bias due to $u_b>u_c$. Therefore, the current immediately flows from T_5 to T_3. T_3 is turned on and does not generate the overlap current. The next commutation is from switch T_3 to switch T_1. During this commutation, the voltage across diode D_1 is u_{ab}, which is positive. Therefore, the current flows immediately from T_3 to T_1 when T_1 is turned on and does not generate the overlap current. The next commutation from T_1 to T_3 will be delayed for overlap time due to the negative voltage of diode D_5, which generates overlap time. Compared with the triangle carrier in Fig. 5(a), the overlap current is reduced. The overlap current occurs thrice in a triangle carrier period but occurs only twice in two positive-going carrier periods.

Similarly, in interval [t_1, t_2], the commutation from T_5 to T_3 will be conducted immediately due to the forward voltage of diode D_3. The next commutation from T_3 to T_1 and from T_1 to

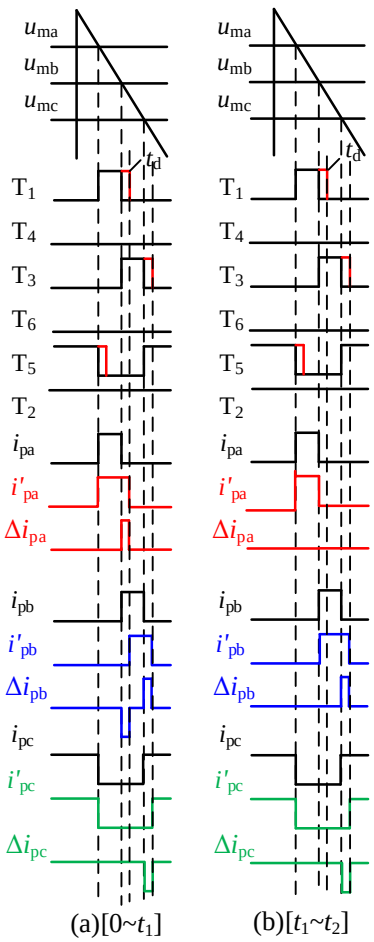

Fig. 8. Current commutation in Sector I (negative-going sawtooth carrier).

T_5 will be delayed for overlap time because diode D_1 bears a reverse voltage. A comparison of Fig. 7 with Fig. 5(a) reveals that the overlap current occurs three times during a triangle carrier period and four times during the two positive-going carrier periods. In this case, the positive-going carrier is unfavorable. The overlap current distributions in the two cases are listed in Tables III and IV, respectively.

On the basis of the distributions in the two tables, some commutation characteristics with positive-going sawtooth carrier can be concluded as follows. The first commutation is from zero state to non-zero state, the second commutation is between non-zero states, and the last commutation is from non-zero state to zero state. Overlap currents exist in the first commutation but are absent in the last commutation. The overlap current in the second commutation depends on the voltage across the diode to be turned on.

The existence of overlap currents in non-zero state is caused by a diode that is under reverse bias and is about to be turned on. As shown in Table III, overlap currents occur when the commutation is from T_3 to T_1. If the commutation is from T_1 to T_3 instead, then the diode to be turned on will be under positive bias and the overlap current will disappear.

TABLE III
OVERLAP CURRENT DISTRIBUTION IN [T0-T1] (POSITIVE-GOING SAWTOOTH CARRIER)

Commutation	Diode to be turned on	Overlap current	Waveform of overlap current
$T_5 \rightarrow T_3$	D_3 : $u_{bc} > 0$	no	no
$T_3 \rightarrow T_1$	D_1 : $u_{ab} > 0$	no	no
$T_1 \rightarrow T_5$	D_5 : $u_{ca} < 0$	Δi_{pa} Δi_{pc}	

TABLE IV
OVERLAP CURRENT DISTRIBUTION IN [T1-T2] (POSITIVE GOING SAWTOOTH CARRIER)

Commutation	Diode to be turned on	Overlap current	Waveform of overlap current
$T_5 \rightarrow T_3$	D_3 : $u_{bc} > 0$	no	no
$T_3 \rightarrow T_1$	D_1 : $u_{ab} < 0$	Δi_{pb} Δi_{pa}	
$T_1 \rightarrow T_5$	D_5 : $u_{ca} < 0$	Δi_{pa} Δi_{pc}	

B. Commutation with Negative-going Sawtooth Carrier

As long as the turn on time of each switch remains unchanged in a carrier cycle, the change of the switching sequence has no influence on the fundamental component of the PWM pulse [14]. Therefore, the negative-slope sawtooth wave can also be adopted as the carrier to modulate the switching sequence.

Fig. 8 illustrates the current commutation in Sector I with the negative-going sawtooth carrier. When the carrier is replaced by a negative slope sawtooth wave (Fig. 8), the distribution of the overlap current will be different from the distribution in Fig. 5(b). According to the relationship of phase bridge voltages in [t_0, t_1] and in [t_1, t_2], the commutation operation in Sector I should be discussed in two cases, $u_a > u_b > u_c$ and $u_b > u_a > u_c$.

In interval [t_0, t_1], the voltage across diode D_3 is positive, and the current flows immediately from T_5 to T_3, which does not produce the overlap current. The next commutation is from switch T_1 to switch T_3. The voltage across diode D_1 is negative voltage u_{ab}. The second commutation from T_1 to T_3 will be delayed for overlap time. So does the commutation from T_3 to T_5. Compared with Fig. 5(b), the overlap current is increased. The overlap current happens three times during a triangle carrier period and four times during two negative-going carrier periods.

In interval [t_1, t_2], both commutations from T_5 to T_1 and T_1 to T_3 occur immediately and do not generate an overlap current. By contrast, the commutation from T_3 to T_5 generates an overlap current for the negative voltage across diode D_5. Compared with Fig. 5(b), the overlap current is reduced. The overlap current occurs thrice during a triangle carrier period and twice during two negative-going carrier periods. The

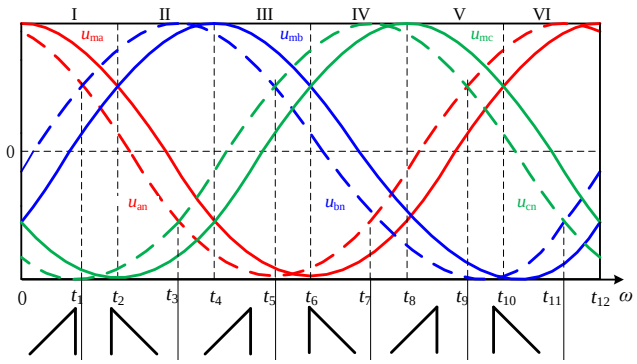

Fig. 9. Distribution of positive-slope and negative-slope sawtooth carriers during one modulation period.

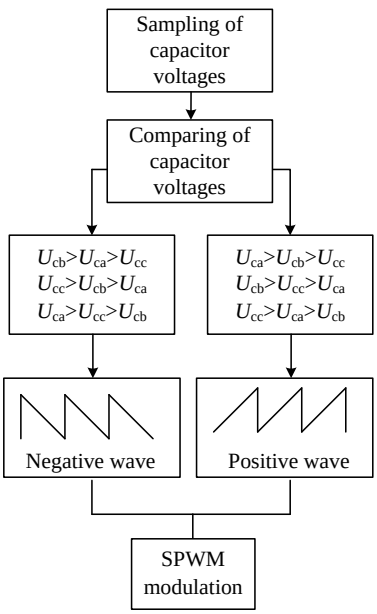

Fig. 10. Control block diagram of overlap current constraining method.

overlap current distribution with negative-going carrier is listed in Tables V and VI.

Figs. 7 and 8 reveal that the overlap currents in $[t_0, t_1]$ can be reduced with positive-going sawtooth carriers, whereas the overlap currents in $[t_1, t_2]$ can be reduced with negative-going sawtooth carriers. Therefore, adopting a negative-slope sawtooth wave as carrier when the diode to be turned on is under reverse bias is a good option.

C. New Overlap Current Restraining Method

A new modulation method is proposed based on the above analysis. The positive-slope and negative-slope sawtooth carriers can be combined to reduce the overlap current, which happens between non-zero states. The type of sawtooth carrier depends on the neutral voltages of phase legs, which can be used to determine the sign of the diode voltage. The key is to make sure the diode to be turned on is in positive bias when commutation occurs between non-zero states.

TABLE V
OVERLAP CURRENT IN [T0, T1] (NEGATIVE-SLOPE SAWTOOTH CARRIER)

Commutation	Diode to be turned on	Overlap current	Overlap current waves
$T_5 \rightarrow T_1$	D_1 : $u_{ac}>0$	no	no
$T_1 \rightarrow T_3$	D_3 : $u_{ba}<0$	Δi_{pa} Δi_{pb}	
$T_3 \rightarrow T_5$	D_5 : $u_{cb}<0$	Δi_{pb} Δi_{pc}	

TABLE VI
OVERLAP CURRENT IN [T1, T2](NEGATIVE-SLOPE SAWTOOTH CARRIER)

Commutation	Diode to be turned on	Overlap current	Overlap current waves
$T_5 \rightarrow T_1$	D_1 : $u_{ac}>0$	no	no
$T_1 \rightarrow T_3$	D_3 : $u_{ba}>0$	no	no
$T_3 \rightarrow T_5$	D_5 : $u_{cb}<0$	Δi_{pb} Δi_{pc}	

Therefore, in Sector I, when $u_a>u_b>u_c$, the positive-slope sawtooth carrier is adopted. When $u_b>u_a>u_c$, the negative-slope sawtooth carrier is adopted. In this way, the overlap current can be prevented when commutation happens between non-zero states. The commutation in other sectors can be analyzed in a similar manner. The distribution of the positive-slope and negative-slope sawtooth carriers during one modulation period is presented in Fig. 9.

The steps for the proposed overlap current restraining method are summarized in Fig. 10. The main operation steps are listed as follows:

1) Sample the grid-side capacitor voltages, namely, the neutral voltages of three phase legs, to determine the voltage of diode to be turned on.
2) Compare the capacitor voltages and choose the suitable sawtooth carrier. When $u_a>u_b>u_c$, $u_b>u_c>u_a$, or $u_c>u_a>u_b$, the positive-slope sawtooth wave will be adopted. When $u_b>u_a>u_c$, $u_c>u_b>u_a$, or $u_a>u_c>u_b$, negative-slope sawtooth wave will be adopted.

Compared with commutation under triangle carriers, the proposed modulation method can reduce the overlap current that happens between non-zero commutation during a triangle carrier period. Therefore, the proposed modulation method can thoroughly restrain the overlap current and effectively reduce the harmonics in the AC-side current of the converter.

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

A. Simulation Verification

To verify the validity of the theoretical analysis, the three-phase current-source rectifier system is established in MATLAB and related simulation results are conducted. The simulation parameters are listed in Table 7.

Due to the influence of overlap currents, extra odd harmonics

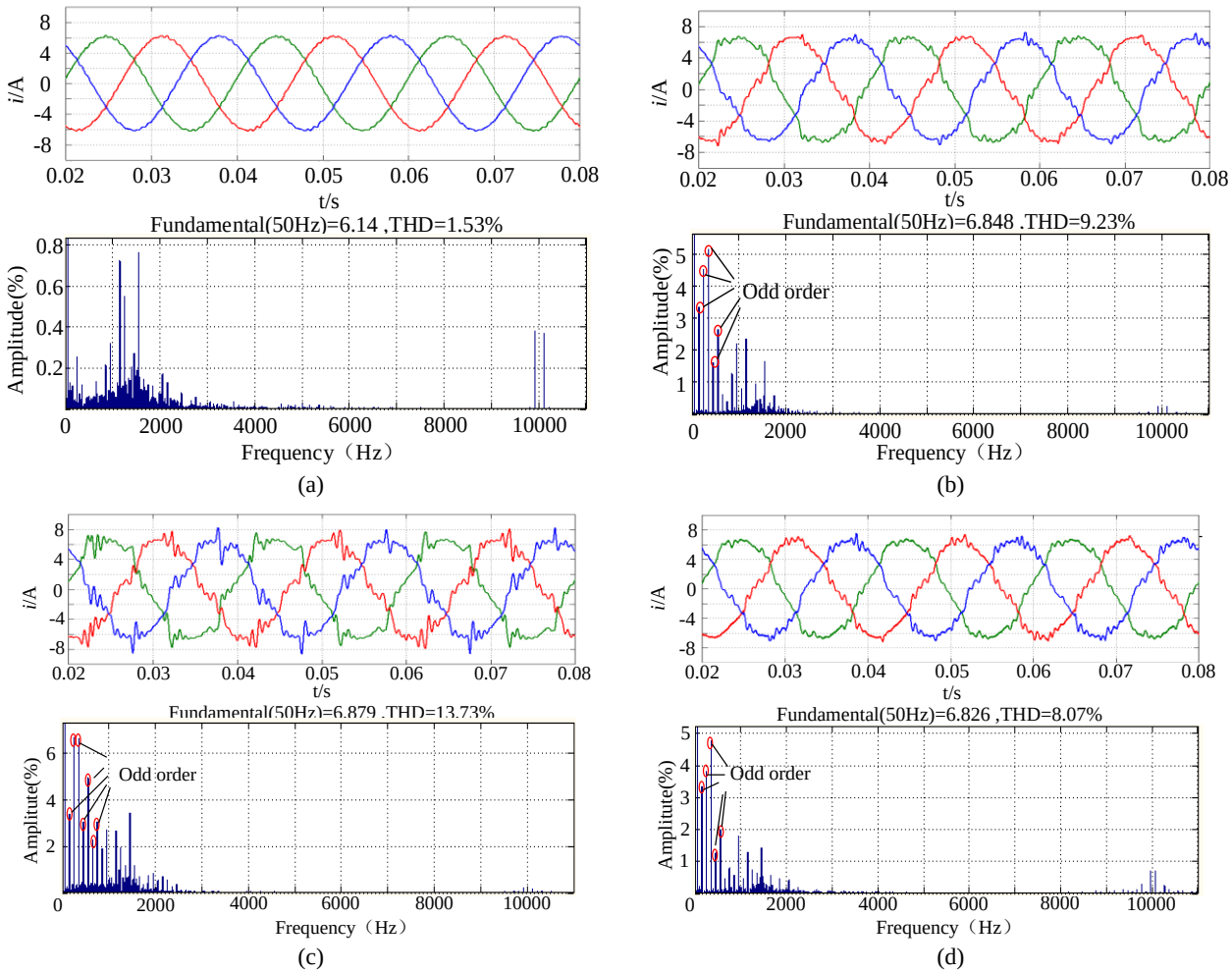

Fig. 11. Waveforms of the grid-side current and FFT analysis. (a) 0 μs overlap time. (b) 5 μs overlap time. (c) 10 μs overlap time. (d) 10 μs overlap time with overlap current constraining method.

TABLE VII
SIMULATION PARAMETERS OF CSR

Parameter	Value
Power/kW	3
Fundamental frequency/Hz	50
Inductance/mH	1.7
Capacitance/μF	10
Switching frequency/kHz	10

are injected into the AC-side currents of the CSR. As analyzed in Section II, the low-order odd harmonics cannot be filtered out by the LC filter and will be amplified by the filter, which leads to the grid-side current distortion. Fig. 11 shows the grid-side current and the total harmonic distortion (THD) analysis waveform with different overlap times. Fig. 11(a) shows that the waveform of the grid-side current is sinusoidal without the overlap time. When the overlap time is added into driving signals, some unexpected influence will occur to the grid-side current. As shown in Figs. 11(b) and 11(c), the harmonic components increase proportionally with overlap time. The THD of grid-side currents is 1.53% without overlap time. When the overlap time is 5 μs, the THD of grid-side currents increases to 9.23%. When the THD of grid-side currents is 10 μs, the THD of AC-side currents increases to 13.73%. The third, fifth, and seventh harmonic components increase greatly as well, which is in agreement with the analysis in Section II that a great amount of odd harmonics as characteristic harmonics will be injected into the AC-side current with added overlap time. However, even non-characteristic harmonics account for a small fraction of total harmonics. The simulation results on even harmonic content with different overlap times are shown in Fig. 12. The even harmonic content is very small and shows few relations with different overlap times. In sum, the third, fifth, and seventh harmonic contents increase greatly and the second- and fourth-order harmonic contents are always kept small. This finding indicates that the overlap time only brings extra odd harmonics to the AC-side current and confirms that the formulas in Section II are reliable.

A comparison of Figs. 11(c) and 11(d) illustrate that the proposed modulation scheme can decrease THD from 13.73% to 8.07%, and the odd harmonics are decreased greatly, which

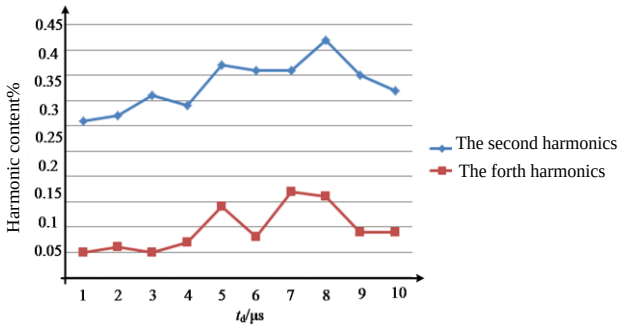

Fig. 12. THD curves of second harmonic and fourth harmonic under different overlap time conditions.

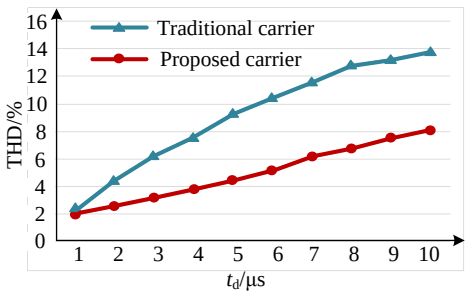

Fig. 13. THD curve of grid-side current before and after adopting the overlap current constraining method.

Fig. 14. 3 kW prototype of the current-source rectifier.

significantly improves the quality of the grid-side current. When the even harmonics slightly change, the second harmonic increases from 0.37% to 0.47% and the fourth harmonic increases from 0.09% to 0.18% with increasing overlap time. When the proposed modulation scheme is performed under 5 μs overlap time, the second harmonic decreases from 0.42% to 0.3% and the fourth harmonic decreases from 0.14% to 0.06%, which indicates that the overlap time has little influence on even harmonics.

Fig. 13 shows the relationship between the THD of grid-side current and overlap time. Under the traditional and proposed carriers, the harmonic contents increase with overlap time. The new modulation method can reduce the THD of grid-side current, and the improvement is noticeable when the overlap time is long. The new modulation method can significantly improve the grid-side current quality.

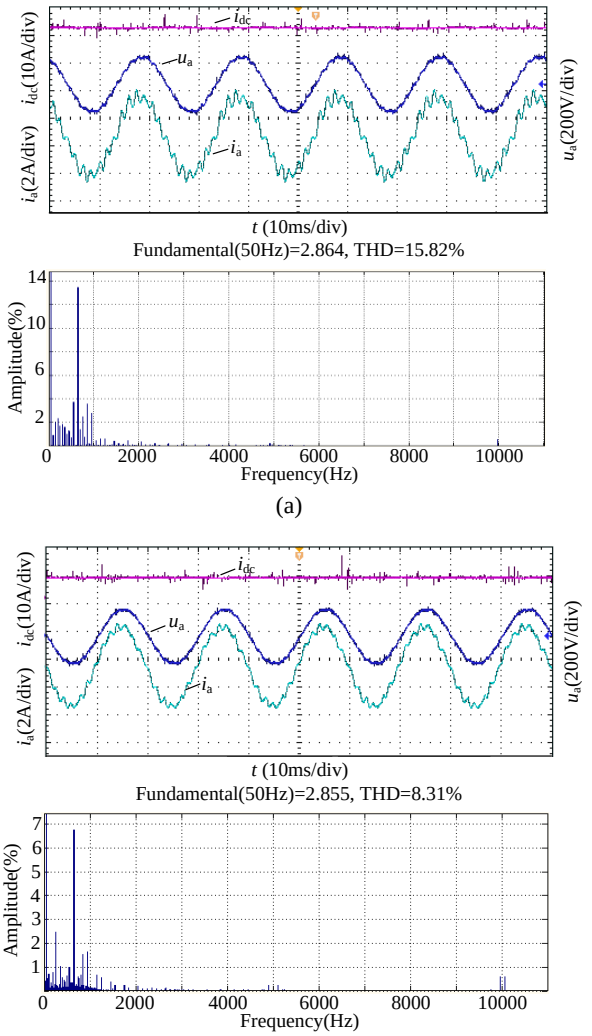

Fig. 15. Experimental waveform of grid current and FFT analysis with the overlap current constraining method. (a) t_d=10μs. (b) t_d=2μs.

B. Experimental Verification

To verify the correctness of the theoretical analysis in Section II and the advantages of the proposed modulation method, a 3 kW experimental prototype is built with the specifications in Table 7. Fig. 14 shows a photograph of the current-source rectifier prototype.

First, the waveform of the grid-side voltage and current conducted under different overlap times and loads are obtained by using traditional modulation methods. Fig. 15(a) shows the grid-side voltage and current waveform of Phase A and harmonics distribution with 10 μs overlap time and 8A DC current, where an apparent current distortion exists in the grid-side current and the THD is 15.82%. Fig. 15(b) is obtained with 2 μs overlap time and 8A DC current, in which the quality of the grid-side current is improved and the THD is reduced to 8.31%.

Fig. 16 shows the THD of the grid current under different

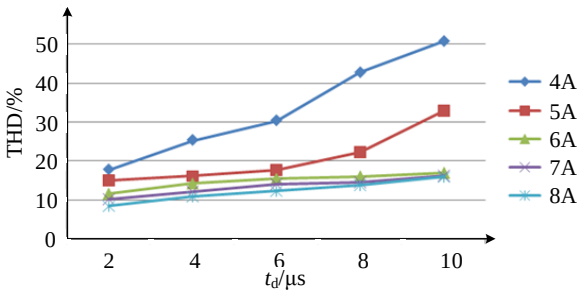

Fig. 16. THD curve of the grid current under different load conditions.

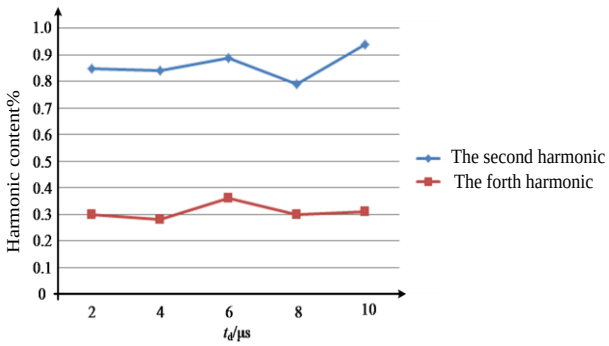

Fig. 17. Content of the second- and fourth-order harmonics under different overlap times.

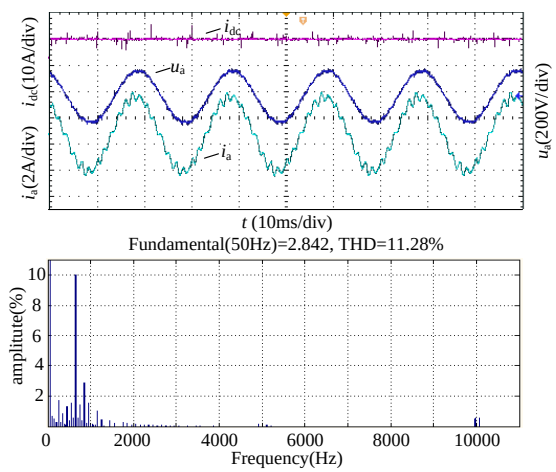

Fig. 18. Waveforms of the grid-side current after using the overlap current constraining method and FFT analysis (t_d=10μs).

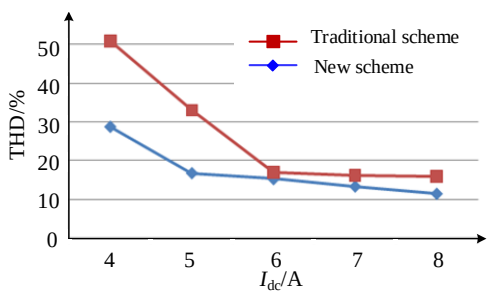

Fig. 19. Relationship of the THD with load current under different modulation methods.

load conditions and overlap times. A comparison of Figs. 15(a) and 15(b) shows the relationship of harmonic content under different DC currents in Fig. 16, where harmonic content increases linearly with overlap time and decreases with load currents, especially the low odd-order harmonic components. Fig. 17 shows the relationship between even order harmonics and overlap time, which indicates that even harmonics as a non-characteristic harmonic are independent of overlap time.

Fig. 18 shows the results with 10 μs overlap time and 8A loads when the overlap current constraining modulation is adopted. Compared with Fig. 15(a), THD decreases from 15.82% to 11.28%, especially the low-order odd harmonics. Moreover, the second harmonic decreases from 0.94% to 0.84%, and the fourth harmonic decreases from 0.31% to 0.29%. When the overlap time is 8 μs with the proposed modulation, the second harmonic increases from 0.79% to 0.81% and the fourth harmonic increases from 0.3% to 0.31%, which indicates that the overlap current constraining method has no influence on the even order harmonics.

Fig. 19 shows the relationship of THD with load current under different modulation methods. The THD of the grid-side current decreases with the increase of load current. The proposed modulation methods can improve the quality of the grid-side current, especially in light loads, which validates the effectiveness of the proposed modulation method.

In summary, the experimental results demonstrate that the overlap current would inject harmonics into the AC-side current, in which the low odd-order harmonics cannot be filtered by the LC filter and would worsen the grid-side current quality. The THD of the grid-side current increases with the overlap time because of the injection of the low odd order harmonics. The even harmonics are independent of the overlap time. The new modulation method can also restrain the overlap current in non-zero commutation and greatly reduce the odd harmonics. Notably, overlap time should also be reduced as much as possible to ensure the grid-side current harmonics meet the relevant standards better.

V. CONCLUSIONS

This paper presents an analysis of the causes and effects of overlap time during a modulation period. To improve the quality of the grid-side current, a new modulation method that combines positive-slope and negative-slope sawtooth carriers is proposed, which can restrain overlap current and improve the AC-side current quality. Simulation and experimental results demonstrate that the odd harmonics can be reduced greatly with the new modulation method.

The detailed conclusions are given as follows:

1) Overlap time brings extra harmonics to the AC-side current. The harmonics consist of low-frequency odd harmonics, which increase proportionally with the overlap time and

cannot be filtered by the LC filter.

2) When the positive and negative slope sawtooth waves are combined to act as the carrier, the new modulation method can effectively restrain the low-frequency current harmonics caused by the overlap time.

3) To ensure the AC-side current meets the relevant standards, in addition to adopting the overlap current harmonic suppression method, the overlap time must also be kept as short as possible.

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REFERENCES

[1] Y. Zhang and Y. W. Li, "Grid harmonics compensation by using high-power PWM converters based on combination approach," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 6431-6438, 2015.

[2] D. Yang, Z. Lu, N. Hang, and G. Li, "Novel quasi direct power control for three-phase voltage-source PWM rectifiers with a fixed switching frequency," in *Proceedings of the Csee*, Vol. 31, pp. 66-73, 2011.

[3] H. Li, X. Zhu, X. Shi, and Y. Peng, "A control scheme of current-source PWM rectifier under unbalanced supply conditions." in *Transactions of China Electrotechnical Society*, Vol. 25, No. 7, pp. 85-92, Jul. 2010.

[4] K. Wei, "Output filter design method in current-source PWM converters," *Transactions of China Electrotechnical Society*, Vol. 27, No. 6, pp. 83-89, Jun. 2012.

[5] B. Guo, F. Wang, and R. Burgos, "Modulation scheme analysis for high efficiency three-phase buck rectifier considering different device combinations." in *IEEE Energy Conversion Congress and Exposition*, pp. 26-33, 2012.

[6] F. Xu, B. Guo, L. M. Tolbert, F. Wang, and B. J. Blalock, "Design and performance of an all-SiC three-phase buck rectifier for high efficiency data center power supplies," in *Energy Conversion Congress and Exposition*, pp. 2927-2933, 2012.

[7] T. B. Soeiro, T. Friedli, and J. W. Kolar, "Design and implementation of a three-phase buck-type third harmonic current injection PFC rectifier SR," *IEEE Trans. Power Electron.*, Vol. 28, No. 4, pp. 1608-1621, Apr. 2013.

[8] B. Wu, J. Pontt, J. Rodriguez, S. Bernet, and S. Kouro. "Current-source converter and cycloconverter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 7, pp. 2786-2797, Jul. 2008.

[9] S. Kouro, J. Rodriguez, B. Wu, S. Bernet, and M. Perez, "Powering the future of industry: high-power adjustable speed drive topologies," *IEEE Ind. Appl. Mag.*, Vol. 18, No. 4, pp. 26-39, Jul./Aug. 2012.

[10] S. Chi, P. Singerl, and C. Vogel, "Coding efficiency optimization for multilevel PWM based switched-mode RF transmitters," in *IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1-4, 2011.

[11] H. Qin, Q. Liu, X. Zhang, Y. Zhang, and D. Wang "Influence of the overlap time on the ac grid current of CSR and its restraining method," in *IECON* 2017, pp. 1249-1254, 2017.

[12] M. H. Ali, B. Wu, and R. A. Dougal, "An overview of SMES applications in power and energy systems," *IEEE Trans. Sustain. Energy*, Vol. 1, No. 1, pp. 38-47, Apr. 2010.

[13] B. Guo, F. Wang, E. Aeloiza, P. Ning, and Z. Liang, "All-SiC power module for delta-type current source rectifier," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4388-439, 2014.

[14] B. Guo, F. Wang, and E. Aeloiza, "A novel three-phase current source rectifier with delta-type input connection to reduce device conduction loss," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1007-101, 2014.

[15] N. Wang, P. Gao, L. Zhang, X. Li, Y. Jia, Z. Yu, and P. Zhao, "Research and simulation on minimized common-mode voltage SVPWM modulation algorithm for voltage source rectifier," *International Conference on Condition Monitoring and Diagnosis (CMD)*, pp. 424-427, 2016.

[16] B. Liu, H. Ben, T. Meng, and Y. Bai, "Harmonic suppression and stability analysis of three-phase VSR with cosine internal model control strategy," in *IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, pp. 1291-1295, 2016.

[17] M. H. Bierhoff and F. W. Fuchs, "Loss minimized pulse width modulation of IGBT current source converters," in *IECON*, pp. 1739-1744, 2006.

[18] T. Halkosaari and H.Tuusa,"Optimal vector modulation of a PWM current source converter according to minimal switching losses," in *Power Electronics Specialists Conference*, pp. 127-132, 2000.

[19] R. M. Tallam, R. J. Kerkman and R. A. Lukaszewski, "Detection of capacitor degradation in LC filters for AC drives," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 121-127, 2014.

[20] X. Zhang, J. Ji, Y. Yu, Z. Liu, and C. Zhang, "Study of low voltage stress space vector PWM control for current source PWM rectifier," in *Proceedings of the CSEE*, pp.144-149, 2004.

[21] F. Xu, B. Guo, L. M. Tolbert, F. Wang, and B. J. Blalock, "An all-SiC three-phase buck rectifier for high-efficiency data center power supplies," *IEEE Trans. Ind. Appl.*, Vol. 49, No. 6, pp. 2662-2673, Nov./Dec. 2013.

[22] J. Liu and Y. Li, "Dead-time influence on output error of voltage source inverter and compensation," *Transactions of China Electrotechnical Society*, Vol. 22, No. 5, pp. 117-122, May 2007.

[23] A. Stupar, T. Friedli, J. Minibock, and J. W. Kolar, "Towards a 99% efficient three-phase buck-type PFC rectifier for 400-V DC distribution systems," *IEEE Trans. Power Electron.* Vol. 27, No. 4, pp. 1732–1744, Apr. 2012.

[24] X. Zhang and C. Zhang, "PWM rectifiers and control methods," in *Machine PRESS*, 2012.

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